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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/499,859	02/07/2000	Mark Held	FORE -58	1830

7590 05/11/2004

EXAMINER
MOLINARI, MICHAEL J

ART UNIT	PAPER NUMBER
2665	

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DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/499,859	HELD ET AL.	
	Examiner	Art Unit	
	Michael J Molinari	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 5,446,730) in view of Dighe et al. (U.S. Patent No. 5,530,695).

3. Referring to claim 1, Lee et al. disclose an apparatus for establishing circuits in an ATM network comprising: a controller for which a user (see column 1, lines 28-39) specifies which requirements can be changed (see Figure 10, #1006), in what order (see Figure 10, #1004, which shows selecting the "next" performance parameter, which shows that the parameters are ordered), and by how much (see column 6, lines 3-18) for every quality of service requirement of a circuit (see column 3, lines 58-67, column 4, lines 1-2 and 35-58, column 6, lines 64-67 and column 7, lines 1-2) which attempts to establish a circuit according to original quality of service requirements (see column 4, lines 43-46), which determines available resources of the ATM network (see column 4, lines 43-46) and which automatically relaxes the original quality of service requirements associated with a circuit for the circuit to be formed in the ATM network with the available resources of the ATM network (see column 4, lines 46-48); and a memory which stores a plurality of different quality of service requirements, said memory connected to the controller for the controller to obtain different quality of service requirements for the

controller to automatically relax the original quality of service requirements with different quality of service requirements (see column 4, lines 35-41), the memory having the different quality of service requirements ordered in terms of priority for the controller to choose when the controller relaxes the original quality of service requirements and attempts to establish the circuit (see column 4, lines 35-41; see Figure 10, #1004, which shows that the parameters are ordered). Lee et al. differ from claim 1 in that they fail to disclose the use of a UPC associated with the circuit. However, the use of UPCs in ATM networks is well known in the art. For example, Dighe et al. teach the use of a UPC approach, which has the advantage of providing a unified and scalable solution to the issue of QoS (see Abstract). One skilled in the art would have recognized the advantage of using UPCs in an ATM network as taught by Dighe et al. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of UPCs in an ATM network as taught by Dighe et al. into the invention of Lee et al. to achieve the advantage of providing a unified and scalable solution to the issue of QoS. Lee et al. differ from claim 1 in that they fail to disclose the use of a controller and a memory having an index. However, the Examiner takes official notice that the use of controllers and memories with indexes in ATM switches are conventional in the art. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to implement the invention of Lee et al. using a controller and a memory with an index.

4. Referring to claim 2, Lee et al. disclose that the controller automatically selectively relaxes the quality of service requirements by choosing a different quality of service requirement (see column 4, lines 46-48).

5. Referring to claim 4, Lee et al. differ from claim 4 in that they fail to disclose that the controller places a flag in the memory for the circuit when the circuit is established with relaxed quality of service requirements. However, the examiner takes official notice that it is conventional in the art for ATM switches to contain tables in memory containing entries for each connection supported by that switch. Such a table would include circuits with relaxed QoS requirements.

6. Referring to claim 5, Lee et al. disclose that the controller periodically reexamines the ATM network resources and attempts to establish the circuit with the original quality of service requirements in the ATM network (see column 5, lines 52-58, and see column 6, lines 64-67 and column 7, lines 1-2).

7. Referring to claim 6, Lee et al. disclose that the controller attempts to establish the circuit with the original quality of service requirements, if the original quality of service requirements of the circuit cannot be satisfied, the controller attempts to establish the circuit with the quality of service requirements in the index according to their priority until quality of service requirements with a higher priority than the quality of service requirements that the circuit is currently established under in the network is found (see column 4, lines 35-48).

8. Referring to claim 8, Lee et al. disclose a method for establishing circuits in an ATM network comprising the steps of: specifying by a user (see column 1, lines 28-39), which requirements can be changed (see Figure 10, #1006), in what order (see Figure 10, #1004, which shows selecting the "next" performance parameter, which shows that the parameters are ordered), and by how much (see column 6, lines 3-18), for every quality of service requirement of a circuit (see column 3, lines 58-67, column 4, lines 1-2 and 35-58, column 6, lines 64-67 and

column 7, lines 1-2); placing the different quality of service requirements in a memory, each with a priority relative to each other and the original quality of service requirements (see Figure 10, #1004); attempting to form a connection in an ATM network satisfying original quality of service requirements (see column 4, lines 43-36); rejecting the formation of the circuit due to resources of the ATM network not being available to meet the original quality of service requirements of the circuit; relaxing automatically the quality of service requirements of the circuit by choosing the different quality of service requirements by a controller, the plurality in terms of different quality of service requirements ordered in terms of priority stored in a memory connected to the controller (see Figure 10, #1004); and creating the circuit in the ATM network subject to the relaxed quality of service requirements (see column 4, lines 43-48). Lee et al. differ from claim 8 in that they fail to disclose the use of a UPC associated with the circuit. However, the use of UPCs in ATM networks is well known in the art. For example, Dighe et al. teach the use of a UPC approach, which has the advantage of providing a unified and scalable solution to the issue of QoS (see Abstract). One skilled in the art would have recognized the advantage of using UPCs in an ATM network as taught by Dighe et al. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of UPCs in an ATM network as taught by Dighe et al. into the invention of Lee et al. to achieve the advantage of providing a unified and scalable solution to the issue of QoS. Lee et al. differ from claim 8 in that they fail to disclose the use of a controller and a memory having an index. However, the Examiner takes official notice that the use of controllers and memories with indexes in ATM switches are conventional in the art. Therefore, it would have been obvious to a

person with ordinary skill in the art at the time of the invention to implement the invention of Lee et al. using a controller and a memory with an index.

1. Referring to claim 9, Lee et al. disclose that the relaxing step includes the step of relaxing automatically and selectively the original quality of service requirements by choosing different quality of service requirements than the original quality of service requirements (see column 4, lines 43-48 and note that initially Routing tries to satisfy requested QoS, but if it fails it then tries to satisfy acceptable QoS).

2. Referring to claim 16, Dighe et al. disclose that the specifying step includes the step of specifying that the requirements of PCR (peak cell rate), SCR (sustainable cell rate) and MBS (maximum burst size) can be changed (see column 3, lines 39-40, column 5, lines 56-67, column 6, lines 1-42, and column 7, lines 25-53).

3. Referring to claim 17, Dighe et al. disclose that the requirements of PCR, SCR, and MRS can be changed (see column 3, lines 39-40, column 5, lines 56-67, column 6, lines 1-42, and column 7, lines 25-53).

9. Claims 7 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Dighe et al. as applied to claims 6 and 14 above, and further in view of Burns et al. (U.S. Patent No. 6,442,132).

10. Referring to claims 7 and 14-15, Lee et al. in view of Dighe et al. differ from claims 7 and 14 in that they fail to disclose that the circuit is an SPVx circuit. However, the use of SPVCs in ATM is well known in the art. For example, Burns et al. teach the use of SPVCs, which have the advantage of being more robust and efficient than PVCs (see column 1, lines 12-39). One skilled in the art would have recognized the advantage of using SPVCs as taught by Burns et al.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of SPVCs as taught by Burns et al. into the invention of Lee et al. in view of Dighe et al. to achieve the advantage of using connections that are more robust and efficient than PVCs.

11. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 5,446,730).

12. Referring to claim 12, Lee et al. differ from claim 12 in that they fail to disclose that, after the recreating step, there is the step of placing a flag in the memory by the controller corresponding with the circuit that is established with relaxed quality of service requirements. However, the examiner takes official notice that it is conventional in the art for ATM switches to contain tables in memory containing entries for each connection supported by that switch. Such a table would include circuits with relaxed QoS requirements.

13. Referring to claim 13, Lee et al. disclose that, after the creating step, there are the steps of re-examining the ATM network resources and attempting to establish the circuit with the original quality of service requirements in the ATM network (see column 5, lines 52-58, column 6, lines 64-67, and column 7, lines 1-2).

14. Referring to claim 14, Lee et al. disclose that, after the attempting to establish step, there is the step of attempting to establish the circuit with the different quality of service requirements in the index according to their priority until different quality of service requirements with a higher priority than the quality of service requirements that the circuit is currently established under in the network is found (see column 4, lines 35-48).

Response to Arguments

15. Applicant's arguments filed 19 April 2004 have been fully considered but they are not persuasive.

16. Applicant has argued that Lee et al. cannot be combined with Dighe et al. However, the examiner has established in prior office actions that he believes that the combination is proper.

17. Applicant has argued that the cited prior art fails to teach which requirements can be changed, in which order, and by how much. However, as outlined above, the examiner takes the position that Lee et al. does teach such limitations.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J Molinari whose telephone number is (703) 305-5742. The examiner can normally be reached on Monday-Thursday 8am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MJM

Michael Joseph Molinari

DUC HO
PRIMARY EXAMINER

5-10-04